Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 3 and 4 are presently pending in the application. Claims 1, 2, and 5 - 7 have been canceled without prejudice from the instant application, for possible pursuit in a future application. As it is believed that claims 3 and 4 are patentable over the cited art in their original form, the claims have not been amended to overcome the references.

In items 4 - 7 of a final Office Action mailed August 4, 2005 (the "**final Office Action**"), claims 6 and 7 were rejected as allegedly being indefinite under 35 U.S.C. § 112, first paragraph. Claims 6 and 7 have been canceled from the instant application, without prejudice.

It is accordingly believed that the pending claims meet the requirements of 35 U.S.C. § 112, first paragraph.

In item 9 of the **final Office Action**, claims 1, 2 and 5 - 7 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 4,821,183 to Hauris ("**HAURIS**") in view of U. S. Patent No. 5,781,750 to Blomgren et al ("**BLOMGREN**").

Claims 1, 2 and 5 - 7 have been canceled from the instant case, without prejudice. As such, it is believed that Applicants' have obviated the above rejection.

Additionally, in item 19 of the **final Office Action**, claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 5,854,913 to Goetz et al ("**GOETZ**"), in view of U. S. Patent No. 5,088,030 to Yoshida ("**YOSHIDA**"), U. S. Patent No. 4,926,323 to Baror et al ("**BAROR**"), "The PowerPC Architecture", 1994 ("**POWERPC**") and K, Short, "Embedded Microprocessor Systems Design", 1998 ("**SYSTEMS DESIGN**").

Applicants respectfully traverse the above rejections.

Applicants' independent claims 3 and 4 each recites, among other limitations:

> **a multiplexer** having a first input, a second input for receiving a 0 value, and a third input receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place;

Additionally, Applicants' claim 3 recites, among other limitations:

> **an adding unit** connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a

> second input connected to said multiplexer, and an output connected to said computation unit; [emphasis added by Applicants]

Similarly, Applicants' independent claim 4 recites, among other limitations:

> **an subtracting unit** connected between said program counter and said computation unit for the relative addresses, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, and an output connected to said computation unit; [emphasis added by Applicants]

The above limitations are described in the specification of the instant application, for example, in paragraphs [0031] - [0034], which states:

> FIG. 2 shows a second embodiment of the invention. In this case, only one instruction counter PC, which is always pointing to the current instruction line, is provided. In addition, a register 12, which contains an instruction length (Opcode length), must be provided in the microprocessor. **An output of the register 12 is fed here to a multiplexer unit MUX, which is controlled by the parameter that designates the respective assembler code. The other input of the multiplexer MUX is occupied by the value "0". An output of the multiplexer MUX is fed to an adding unit Add, the other input of the adding unit Add is connected to the instruction counter PC.** An output of the adding unit Add is then connected to the computation unit 10 for the relative addresses.
>
> FIG. 3 shows a third embodiment of the invention. In this case, the register 12 that contains the length of an assembler instruction (Opcode length) is likewise provided. **Here, too, the output of the register 12 is fed to the multiplexer unit MUX, which is controlled by the parameter that designates the respective assembler code. Here, too, the other input of the multiplexer unit MUX is occupied by the value 0.**

> **By contrast with the embodiment of FIG. 2, here, however, the output of the multiplexer unit MUX is connected to a subtracting unit Sub.** The other input of the subtracting unit sub is connected to the instruction counter PCnext. In this case, however, the instruction counter PCnext does not point to the current assembler instruction line, but to the next assembler instruction.
>
> Here, too, the output of the subtracting unit Sub is connected to the computation unit 10 for the relative address computation. [emphasis added by Applicants]

The references cited in the **final Office Action** alone, or in combination, neither teach, nor suggest, all limitations of Applicants' claims 3 and 4, including Applicants' particularly claimed multiplexer and/or Applicants' particularly claimed adding unit (claim 3), and subtracting unit (claim 4).

More particularly, item 21 of the **final Office Action**, states:

> While Goetz does teach multiple instruction sets being implemented and indicated by a parameter, Goetz is silent on how the different offsets for branch instructions are handled. It is well known in the art that PowerPC branch instructions add an offset to the address of the branch instruction (Page 36, numeral 1, The PowerPC Architecture), while x86 branch instructions add an offset to the address of the instruction following the branch instruction (Short, Embedded Microprocessor Systems Design, page 190, 2nd paragraph). **However, since Goetz is silent on how the above issue is resolved, Goetz fails to teach:**
>
> > **-A multiplexer having a first input a second input for receiving a zero value, a third input receiving a parameter designating a respective assembler code, a memory for storing an instruction length having an output connected to said first input of said multiplexer**

> **-An addition unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input for an instruction length, and an output connected to said computation unit:** [emphasis added by Applicants]

Rather, the **final Office Action** alleges that a combination of features from **YOSHIDA** and **BAROR**, taken in combination, allegedly disclose the elements missing from **GOETZ**, but needed to teach or suggest Applicants' invention of claims 3 and 4. Applicants respectfully disagree.

Rather, as stated above, Applicants' claimed invention supply an instruction code length from the additional register 12 (see Fig. 2) to a multiplexer, at the second input of which the alternative value "0" is present. If the assembler code is valid, as signaled via the third input, the multiplexer supplies an adding unit (claim 3) or a subtracting unit (claim 4) with either the command word length or the value "0". Contrary to Applicants' claimed invention, **a complicated cascade of adding units** is necessary in **YOSHIDA**, **in order to compute the correct value for determining the relative address on the basis of the program code**. Thus, **YOSHIDA**, like **GOETZ** fails to teach or suggest, among other limitations of Applicants' claims, the controlled supplying of instruction word lengths or the value "0", **to a multiplexer**, **in dependence upon which assembler code is selected**. In lieu of pointing to

such limitation in **YOSHIDA**, the **final Office Action** alleges, in part, in item 24:

> One of ordinary skill in the art would have recognized **that since the purpose of the 1st adder of Yoshida is to add the length** of the branch instruction in order to complete the branch instruction that adds an offset to the address of the instruction following the branch instruction, **it would have been obvious to simply add a zero as said "Word Length" offset to calculate a PowerPC branch target address.** However, Goetz in view of Yoshida fails to teach that the "Word Length" values are stored in a memory and selected via a multiplexer with said parameter as an input. [emphasis added by Applicants]

Applicants' respectfully disagree. The law recognizes that there must be a clear motivation to modify a reference. Absent impermissible hindsight reconstruction of Applicants' invention **YOSHIDA** does not provide such a motivation. Further, making the assumption made in the **final Office Action**, and setting a Word Length Offset to zero **at the first adder of YOSHIDA**, still does not teach or suggest Applicants' particularly claimed **multiplexer** (i.e., **"a multiplexer** having a first input, a second input for receiving a 0 value, and a third input receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place"). As such, it is believed that **YOSHIDA**, alone or in combination with **GOETZ** (and as will be shown below, with **BAROR**), **fails to teach or suggest Applicants' particularly claimed hardware combination, recited in claims 3 and 4.**

Further, the **final Office Action** cites **BAROR** as allegedly disclosing certain limitations of Applicants' claims, missing from **GOETZ** and **YOSHIDA**. However, **GOETZ** and **YOSHIDA**, even taken in combination with **BAROR**, still does not teach or suggest all limitations of Applicants claims 3 and 4.

More particularly, although **BAROR** appears to provide a fixed wiring of instruction word lengths, Applicants believe that **BAROR** fails to teach or suggest the controlled supplying of instruction word lengths or the value "0", to a multiplexer, in dependence upon which assembler code is selected, as recited by Applicants' claims. Applicants' particularly claimed multiplexer limitation is additionally missing from **GOETZ** (as stated in the **final Office Action**) and **YOSHIDA** (as described above). As such, the subject matter of Applicants' claims would not be obvious, even upon combining **GOETZ**, **YOSHIDA**, and **BAROR**. The **POWERPC** and **SYSTEM DESIGN** literature, cited in the **final Office Action**, do not cure the deficiencies of **GOETZ**, **YOSHIDA** and **BAROR**.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 3 and 4. Claims 3 and 4 are, therefore, believed to be patentable over the art.

In view of the foregoing, reconsideration and allowance of claims 3 and 4 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

The instant Preliminary Amendment is being filed simultaneously with a Request for Continuing Examination and a Petition for a Three Month Extension of Time, as the required fees under 37 C.F.R. § 1.17.

Please provide any additional extensions of time that may be necessary and charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, P.A., No. 12-1099.

Respectfully submitted,

For Applicants

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